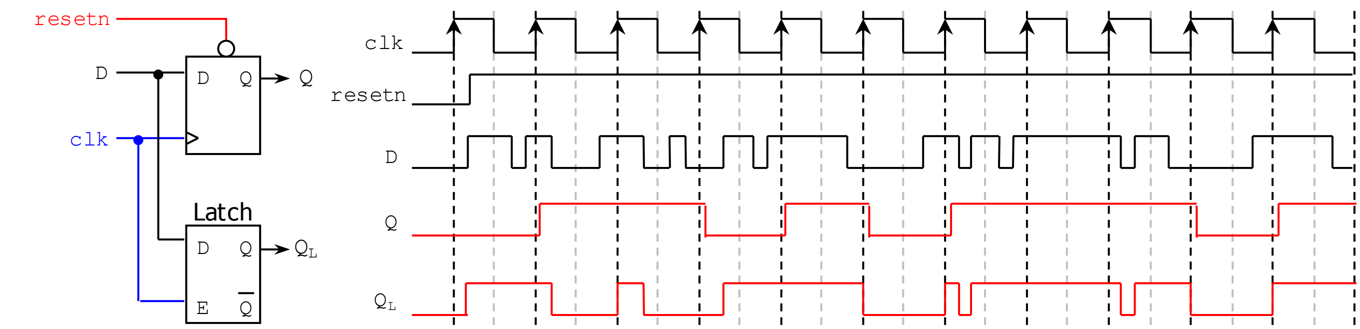
Solutions - Final Exam

(December 14th @ 7:00 pm)

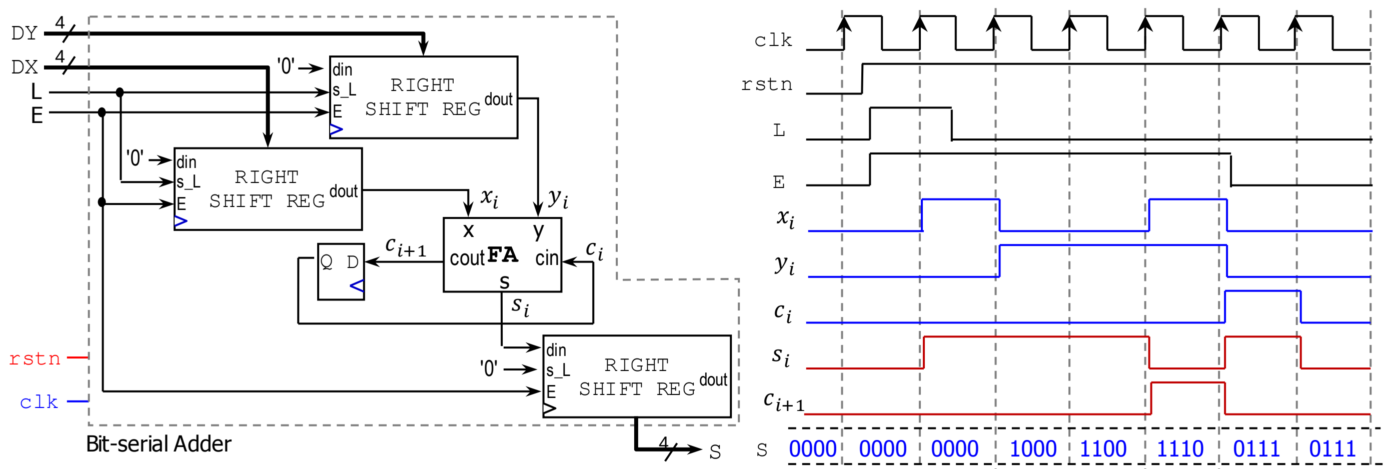
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (18 PTS)

- Complete the timing diagram of the circuit shown below. (8 pts)

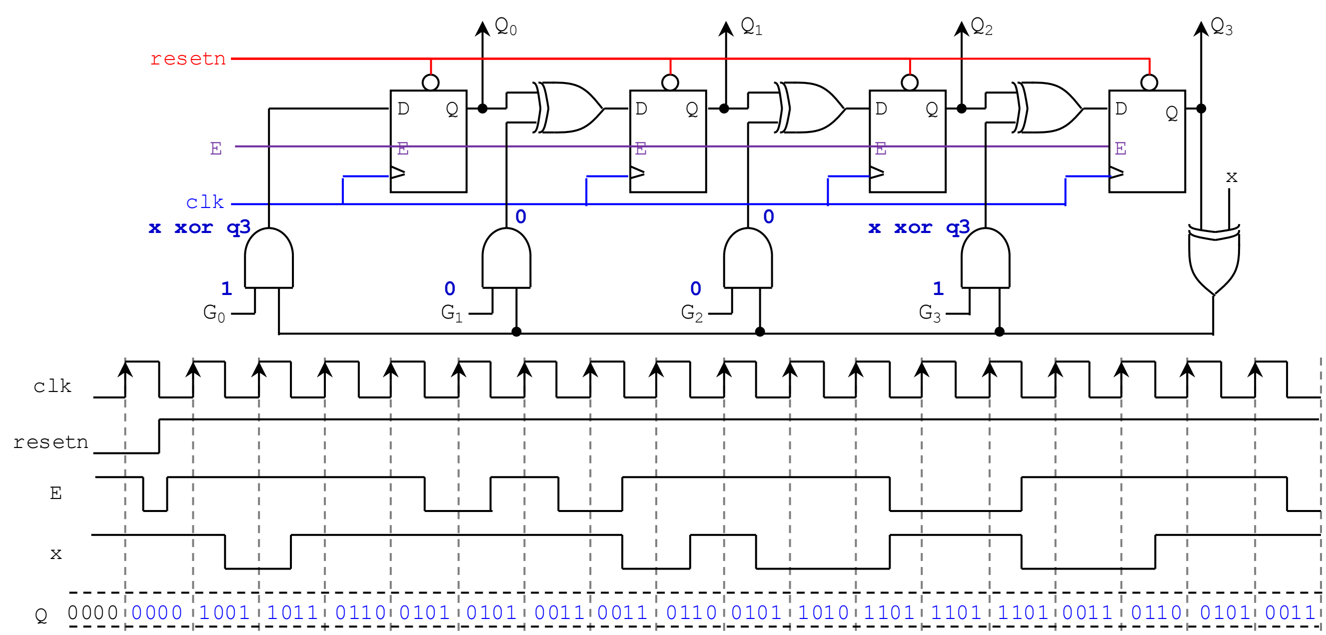


- Complete the timing diagram of the following bit-serial adder. DX=1001, DY=1110. (10 pts)
    - ✓ This circuit includes three 4-bit parallel access shift registers, a flip flop, and a full adder.



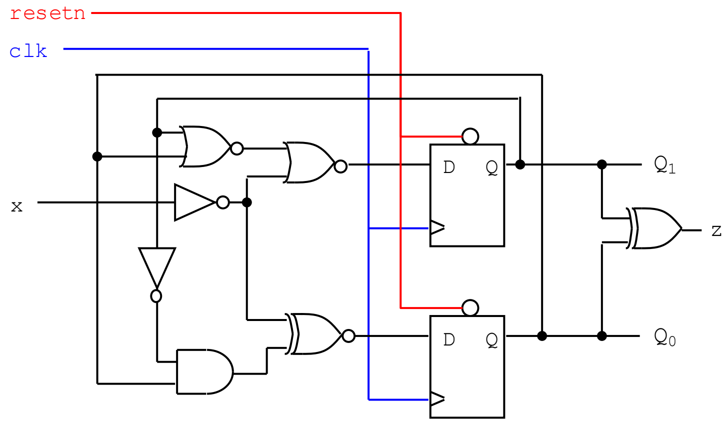
PROBLEM 2 (13 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$



PROBLEM 3 (13 PTS)

- Given the following circuit that represents a Finite State Machine, provide: (12 pts)
  - ✓ Excitation equations and output Boolean equation.
  - ✓ Excitation Table, State Table.
  - ✓ State Diagram (any representation).
- Is this a Mealy or a Moore Machine? (1 pt.)

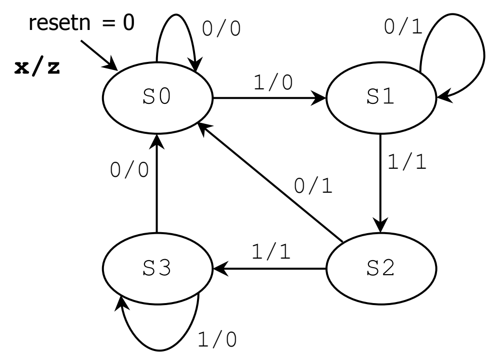


$$Q_1(t+1) \leftarrow (Q_1(t)+Q_0(t))x$$
$$Q_0(t+1) \leftarrow \left(\overline{Q_1(t)Q_0(t)}\right) \oplus x$$
$$z = Q_1(t) \oplus Q_0(t)$$

State assignment: S0: Q=00 S1: Q=01 S2: Q=10 S3: Q=11

x	PRESENT STATE $Q_1Q_0(t)$	NEXTSTATE $Q_1Q_0(t+1)$	z
0	0 0	0 0	0
0	0 1	0 1	1
0	1 0	0 0	1
0	1 1	0 0	0
1	0 0	0 1	0
1	0 1	1 0	1
1	1 0	1 1	1
1	1 1	1 1	0

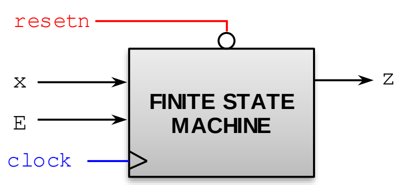
x	PRESENT STATE	NEXT STATE	z
0	S0	S0	0
0	S1	S1	1
0	S2	S0	1
0	S3	S0	0
1	S0	S1	0
1	S1	S2	1
1	S2	S3	1
1	S3	S3	0

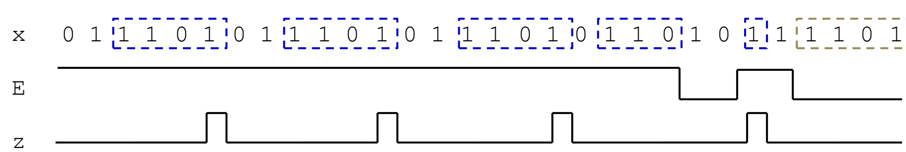


This a Moore FSM.

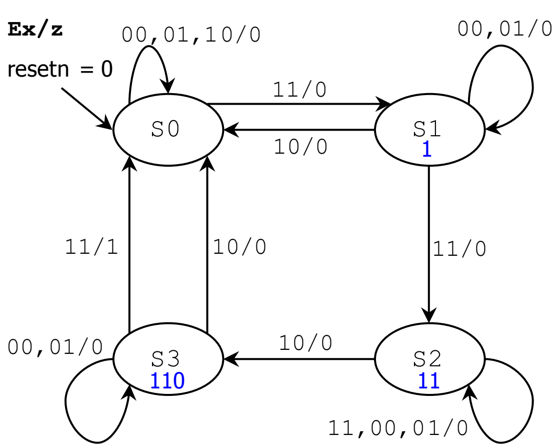
PROBLEM 4 (16 PTS)

- Sequence detector: The machine generates $z=1$ when it detects the sequence 1101. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x, i.e., if E=1, x is valid, otherwise x is not valid.





- Draw the State Diagram (any representation) of this circuit with inputs E and x and output z. (7 pts.)
- Complete the State Table and the Excitation Table. (8 pts.)
- Is this a Mealy or a Moore machine? Why?



E	x	PRESENT STATE	NEXT STATE	z
0	0	S0	S0	0
0	0	S1	S1	0
0	0	S2	S2	0
0	0	S3	S3	0
0	1	S0	S0	0
0	1	S1	S1	0
0	1	S2	S2	0
0	1	S3	S3	0
1	0	S0	S0	0
1	0	S1	S0	0
1	0	S2	S3	0
1	0	S3	S0	0
1	1	S0	S1	0
1	1	S1	S2	0
1	1	S2	S2	0
1	1	S3	S0	1

E	x	PRESENT STATE $Q_1Q_0(t)$	NEXTSTATE $Q_1Q_0(t+1)$	z
0	0	0 0	0 0	0
0	0	0 1	0 1	0
0	0	1 0	1 0	0
0	0	1 1	1 1	0
0	1	0 0	0 0	0
0	1	0 1	0 1	0
0	1	1 0	1 0	0
0	1	1 1	1 1	0
1	0	0 0	0 0	0
1	0	0 1	0 0	0
1	0	1 0	1 1	0
1	0	1 1	0 0	0
1	1	0 0	0 1	0
1	1	0 1	1 0	0
1	1	1 0	1 0	0
1	1	1 1	0 0	1

State assignment: S0: Q=00 S1: Q=01 S2: Q=10 S3: Q=11

This a Mealy FSM. The output z depends on the inputs and the present state.

PROBLEM 5 (18 PTS)

- "Counting 0's" Circuit: It counts the number of bits in register A that has the value of '0'.
  - ✓ Example: for $n = 8$: if $A = 00110010$, then $C = 0101$.
  - ✓ The behavior (on the clock tick) of the generic components is as follows:

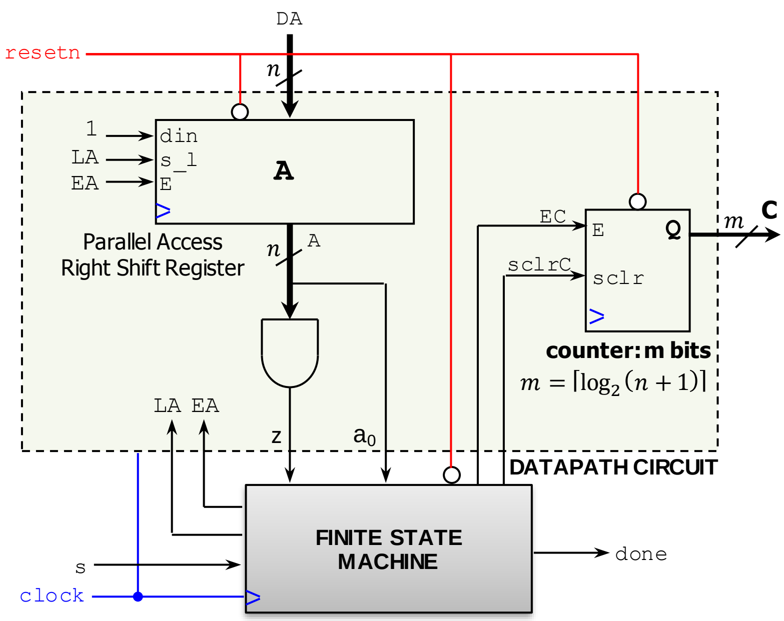
m-bit counter (modulo-n+1): If E=0, the count stays.

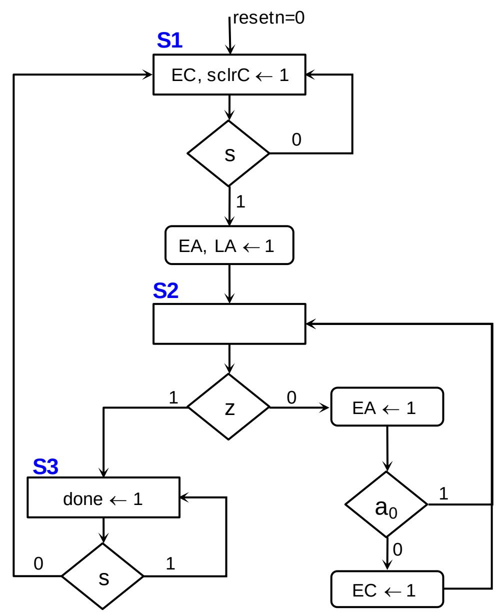
```
if E = 1 then
   if sclr = 1 then
      Q ← 0
   else
      Q ← Q+1
  end if;
end if;
```

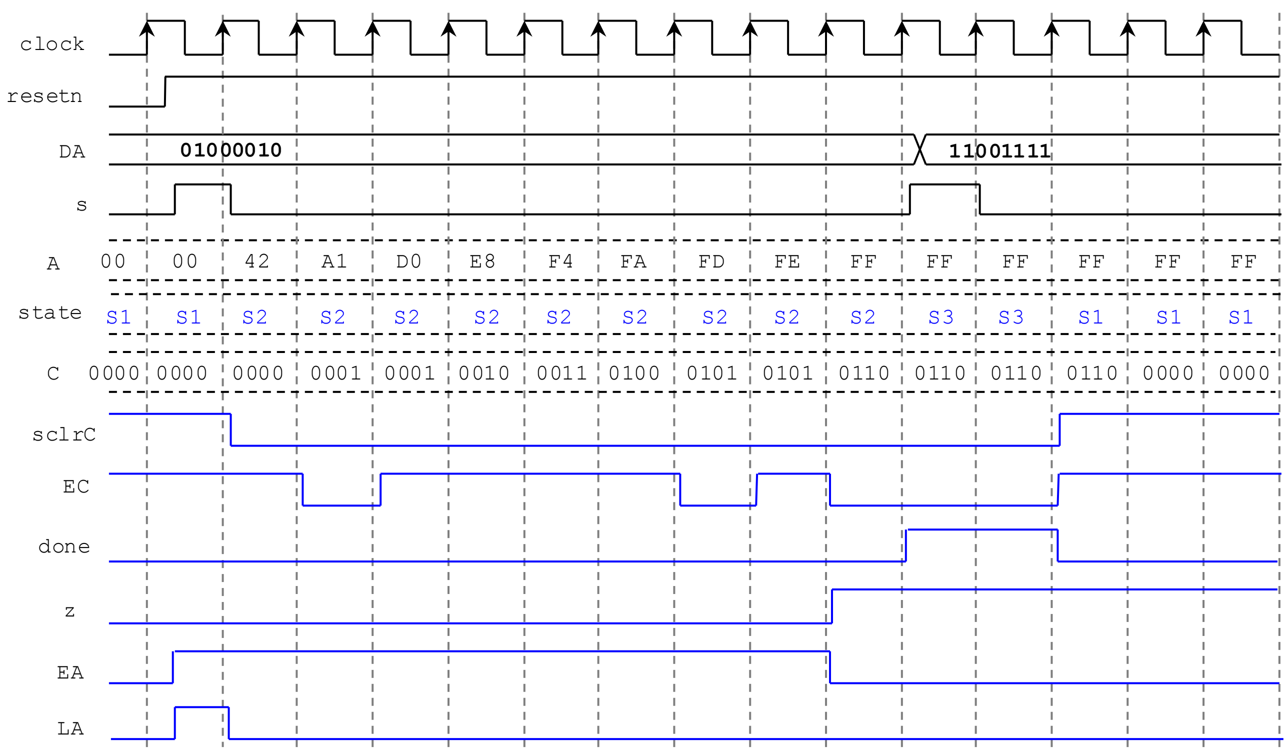
n-bit Parallel access shift register: If E=0, the output is kept.

```
if E = 1 then
   if s_l = '1' then
      Q ← D
   else
      Q ← shift in 'din'  (to the right)
  end if;
end if;
```

- Complete the timing diagram where $n = 8, m = 4$. A is represented in hexadecimal format, while C is in binary format.





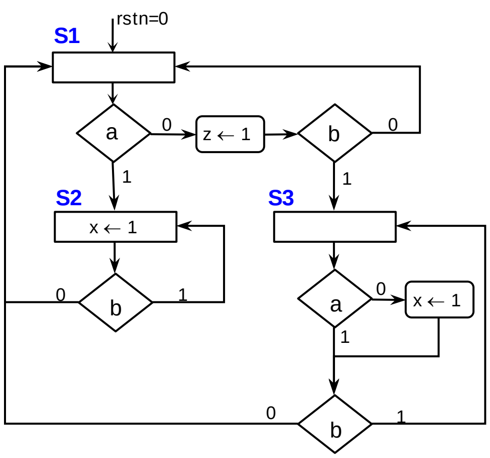


PROBLEM 6 (22 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. (6 pts)
- Provide the State Table and the Excitation Table. Is it a <u>Mealy</u> or a <u>Moore</u> FSM? (6 pts).
- Provide the excitation equations and the Boolean output equations (simplify your circuit: K-maps or Quine-McCluskey).
- Sketch the circuit. (3 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, rstn: in std_logic;
          a, b: in std_logic;
          x, z: out std_logic);
end circ;
```




```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (rstn, clk, a, b)
  begin
     if rstn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
           when S1 =>
               if a = '1' then
                  y <= S2;
               else
                 if b = '1' then y <= S3; else y <= S1; end if;
               end if;
            when S2 =>
               if b = '1' then y <= S2; else y <= S1; end if;
            when S3 =>
               if b = '1' then y <= S3; else y <= S1; end if;
         end case;
      end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; z <= '0';
      case y is
         when S1 => if a = '0' then z <= '1'; end if;
         when S2 => x <= '1';
         when S3 => if a = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```

- State Table and Excitation Table:

a	b	PRESENT STATE	NEXT STATE	x	z
0	0	S1	S1	0	1
0	0	S2	S1	1	0
0	0	S3	S1	1	0
0	1	S1	S3	0	1
0	1	S2	S2	1	0
0	1	S3	S3	1	0
1	0	S1	S2	0	0
1	0	S2	S1	1	0
1	0	S3	S1	0	0
1	1	S1	S2	0	0
1	1	S2	S2	1	0
1	1	S3	S3	0	0

PRESENT STATE				NEXTSTATE			
a	b	Q_1	Q_0 (t)	Q_1	Q_0 (t+1)	x	z
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0
0	0	1	1	X	X	X	X
0	1	0	0	1	0	0	1
0	1	0	1	0	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	X	X	X	X
1	0	0	0	0	1	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	X	X	X	X
1	1	0	0	0	1	0	0
1	1	0	1	0	1	1	0
1	1	1	0	1	0	0	0
1	1	1	1	X	X	X	X

State assignment:
S1: Q=00
S2: Q=01
S3: Q=10

This a Mealy FSM. The outputs x and z depend on the input as well as on the present state.

- Minimization, Excitation equations (including Boolean output equations), and circuit implementation:

$Q_1(t+1) \leftarrow bQ_1(t) + \bar{a}b\overline{Q_0(t)}$
$Q_0(t+1) \leftarrow a\overline{Q_1(t)}.\overline{Q_0(t)} + bQ_0(t)$
$x = Q_0(t) + \bar{a}Q_1(t)$
$z = \bar{a}\overline{Q_1(t)}.\overline{Q_0(t)}$

$Q_1(t+1)$

Q_1Q_0 \ ab	00	01	11	10
00	0	1	0	0
01	0	0	0	0
11	X	X	X	X
10	0	1	1	0

$Q_0(t+1)$

Q_1Q_0 \ ab	00	01	11	10
00	0	0	1	1
01	0	1	1	0
11	X	X	X	X
10	0	0	0	0

x

Q_1Q_0 \ ab	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	X	X	X	X
10	1	1	0	0

z

Q_1Q_0 \ ab	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	X	X	X	X
10	0	0	0	0